CLAIMS:

1. A method of forming an insulative material along a conductive structure, comprising:

providing a conductive structure over a substrate;

forming an electrically insulative material along at least a portion of the conductive structure, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

forming a dopant barrier layer over the electrically insulative material; and

forming a doped oxide material over the dopant barrier layer, the dopant barrier layer preventing dopant migration from the doped oxide material to the electrically insulative material.

2. The method of claim 1 wherein the electrically insulative material is formed to a thickness of at least about 50Å.

3. The method of claim 1 wherein the electrically insulative material consists essentially of the $Si_xO_yN_z$.

4. The method of claim 1 wherein the electrically insulative material consists essentially of the $Si_xO_yN_z$ and is against the conductive structure.

5. The method of claim 1 wherein the electrically insulative material consists essentially of the Al_pO_q.

6. The method of claim 1 wherein the electrically insulative material consists essentially of the Al_pO_q and is against the conductive structure.

7. The method of claim 1 wherein the forming the dopant barrier layer comprises chemical vapor depositing silicon oxide from a TEOS precursor.

8. The method of claim 1 wherein the doped oxide material comprises BPSG.

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9. A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall; the electrically insulative material comprising at least two separate layers; the at least two layers having different chemical compositions from one another; a first of the at least two layers comprising at least one of $Si_xO_yN_z$ or Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10; a second of the at least two layers consisting essentially of silicon and nitrogen; and

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall; the anisotropically etching comprising etching both of the first and second of the at least two layers.

10. The method of claim 9 further comprising implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant.

11. The method of claim 9 wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall.

12. The method of claim 9 wherein the first of the at least two layers consists essentially of the $Si_xO_yN_z$ and is between the second of the at least two layers and the transistor gate sidewall.

13. The method of claim 9 wherein the first of the at least two layers consists essentially of the Al_pO_q and is between the second of the at least two layers and the transistor gate sidewall.

14. A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming source/drain regions within the substrate and proximate the transistor gate;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

chemical vapor depositing silicon oxide over the transistor gate and electrically conductive material utilizing a TEOS precursor; and

forming BPSG over the silicon oxide, the BPSG being spaced from the electrically insulative material of the spacer by the silicon oxide.

15. The method of claim 14 wherein the electrically insulative material is formed to extend across a top of the transistor gate.

16. The method of claim 14 wherein the electrically insulative material consists of Al_2O_3.

17. The method of claim 14 wherein the electrically insulative material consists of aluminum and oxygen.

18. The method of claim 14 wherein the electrically insulative material consists of silicon, nitrogen and oxygen.

19. A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall;

implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant;

chemical vapor depositing silicon oxide over the transistor gate and spacer utilizing TEOS as a precursor of the silicon oxide; and

forming BPSG over the silicon oxide, the BPSG being spaced from the electrically insulative material of the spacer by the silicon oxide.

20. The method of claim 19 wherein the electrically insulative material comprises to different layers that are against one another, one of the layers consisting of silicon nitride, and the other of the two layers consisting of either the $Si_xO_yN_z$ or the Al_pO_q.

21. A transistor structure, comprising:

a semiconductive substrate;

a transistor gate over the substrate, the transistor gate having a sidewall which comprises electrically conductive material;

source/drain regions within the substrate and proximate the transistor gate;

an electrically insulative material along the electrically conductive material of the sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

a layer consisting of silicon dioxide over the transistor gate, electrically insulative material, and substrate; and

a layer of BPSG over the layer consisting of silicon dioxide.

22. The structure of claim 21 wherein the electrically insulative material extends across a top of the transistor gate.

23. The structure of claim 21 wherein the electrically insulative material does not extend across a top of the transistor gate.

24. The structure of claim 21 wherein the electrically insulative material does not extend across a top of the source/drain regions.

25. The structure of claim 21 wherein the electrically insulative material consists of aluminum and oxygen.

26. The structure of claim 21 wherein the electrically insulative material consists of Al_2O_3.

27. The structure of claim 21 wherein the electrically insulative material consists of silicon, nitrogen and oxygen.

28. The structure of claim 21 wherein the electrically insulative material comprises a layer of silicon nitride against a layer of the $Si_xO_yN_z$.

29. The structure of claim 21 wherein the electrically insulative material comprises a layer of silicon nitride against a layer of the Al_pO_q.

30. A transistor structure, comprising:

a substrate;

a transistor gate over the substrate, the transistor gate having a sidewall which comprises electrically conductive material;

source/drain regions within the substrate and proximate the transistor gate;

an electrically insulative pillar along the electrically conductive material of the sidewall, the pillar comprising a first material against a second material, one of the first and second materials comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

a layer consisting of silicon dioxide over the transistor gate, pillar and substrate; and

a layer of BPSG over the layer consisting of silicon dioxide.

31. The structure of claim 30 wherein the first material is silicon nitride and the second material is silicon oxynitride.